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06ES33

# Third Semester B.E. Degree Examination, Dec.09/Jan.10
# Logic Design

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer any FIVE full questions, selecting at least TWO questions from each part.***



## PART – A

1 a. Show that y = f (ABCD) = $\sum$ (0, 2, 5, 7, 8, 10, 13,15) is the complement of y = f(ABCD) = $\pi$(1, 3, 4, 6, 9, 11, 12, 14). Illustrate your answer using Karnaugh map to show the complement nature of the two equations. Realize both the functions using 7486 IC chip [Exclusive OR gates] only. **(12 Marks)**

b. Design a logic circuit that controls the passage of a signal 'A' according to the following requirement.
   i) Output 'X' will equal 'A' when control inputs B and C are the same.
   ii) 'X' will remain 'HIGH' when B and C are different
   Implement the circuit using suitable gates. **(08 Marks)**

2 a. Simplify the following expression using Quine- McClusky technique. Implement the simplified circuit using basic gates: f (ABCD) = $\sum$ (1, 3, 4, 5, 6, 9, 11, 12, 13, 14). **(12 Marks)**

b. Simplify the following Boolean expression using VEM technique. [3 variable map].
   f (ABCD) = $\sum$m (0, 4, 5, 6, 13, 14, 15) + dc (2, 7, 8, 9)

| A | B | C | D | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | $\phi$ |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | $\phi$ |

| A | B | C | D | f |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | $\phi$ |
| 1 | 0 | 0 | 1 | $\phi$ |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

$\phi$ = don't care term. **(08 Marks)**

3 a. Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active HIGH enable and active low data outputs. Use such a decoder to realize the full adder circuit. **(08 Marks)**

b. Design a suitable BCD adder circuit using 74LS83 and a provision has to be made for self correction in case if the sum is not a valid BCD number format. **(12 Marks)**

4 a. Implement the following Boolean function using 4 :1 MUX
   y (ABCD) = $\sum$m (0, 1, 2, 4, 6, 9, 12, 14). **(10 Marks)**

b. Design a circuit that accepts 2 unsigned 4 bit numbers and provides 3 outputs. The inputs are $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$. Outputs are A = B, A > B and A < B. Draw the logic diagram. **(10 Marks)**

## PART – B

5 a. Explain the following:
   i) Switch debouncing and it's elimination
   ii) Race around problem and its elimination. **(14 Marks)**

   b. Obtain the characteristic equation for the following flip flops:
   i) JK flip flop
   ii) SR flip flop. **(06 Marks)**

6 a. With the help of a diagram, explain the following with respect to shift register:
   i) Parallel in and serial out
   ii) Ring counter and twisted ring counter. **(08 Marks)**

   b. Design a Mod – 5 synchronous counter using JK flip flop. **(12 Marks)**

7 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. **(10 Marks)**

   b. A sequential circuit has one input and one output. The state diagram is as shown in Fig.7(b). Design a sequential circuit with 'T' flip flop. **(10 Marks)**

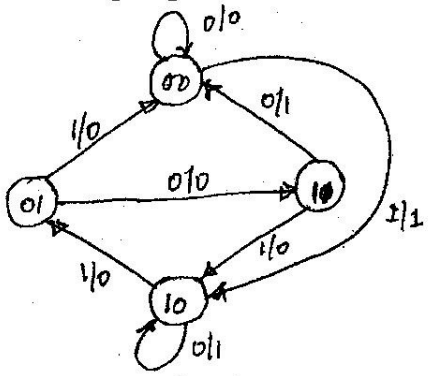


Fig.7(b).

8 a. Analyse the following sequential circuit shown in Fig.8(a) and obtain:
   i) Flip flop input and output equations.
   ii) Transition equation
   iii) Transition table
   iv) State table
   v) Draw the state diagram. **(12 Marks)**

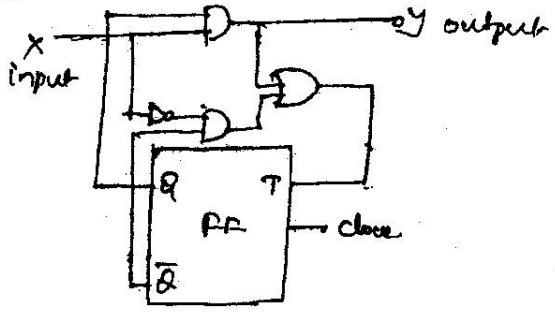


Fig.8(a).

   b. With a suitable example and appropriate state diagram, explain how to recognize a particular sequence. Ex: 1011. (Any sequence can be assumed). **(08 Marks)**

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